IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:　　　　　　　　）

Katsuhiko HIEDA et al.　　　　　　　）

Serial No.:　09/469,190　　　　　　）　　Group Art Unit:　2812

Filed:　December 21, 1999　　　　　）　　Examiner:　Unassigned

For:　SEMICONDUCTOR DEVICE　　）
　　　AND METHOD FOR　　　　　　）
　　　MANUFACTURING THE SAME　）

Assistant Commissioner for Patents
Washington, D.C.　20231

Sir:

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MAY 23 2000
TC 2800 MAIL ROOM

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97(b)

This Supplemental Information Disclosure Statement (IDS) is being filed to correct a typographical error in the IDS filed March 31, 2000. That IDS incorrectly cited co-pending application serial no. 09/364,174. However, the correct serial no. of the co-pending application which applicants wish to bring to the Examiner's attention is 09/369,174.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that the above-noted co-pending application is material or constitutes "prior art." If the Examiner applies the document as prior art against any claim in the application and Applicants determine that the cited document does not constitute "prior art" under United States law, Applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of the document.
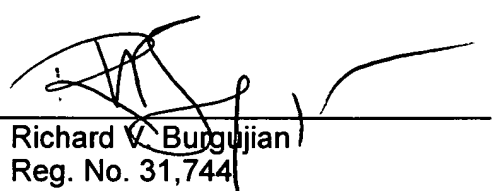
Not Consider

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the co-pending application, should it be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By:_____
Richard V. Burgujian
Reg. No. 31,744

Date: May 18, 2000

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